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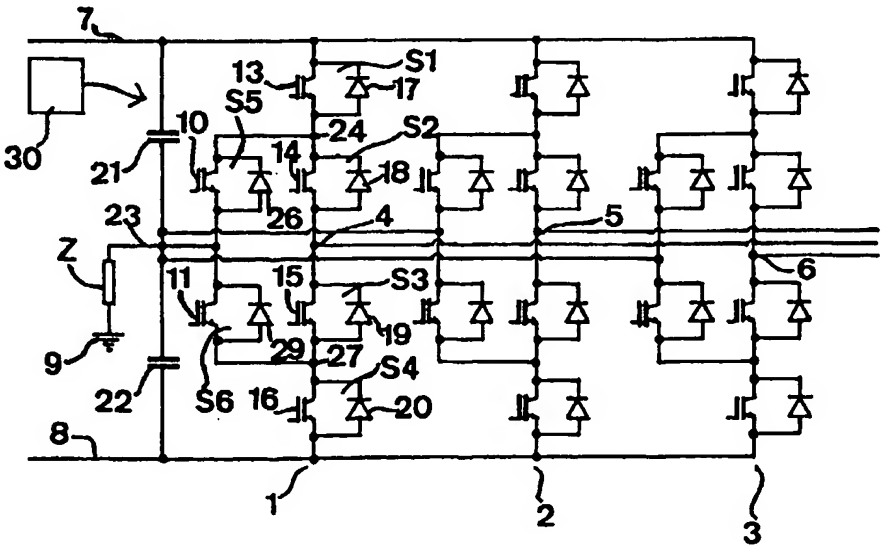
(54) Title: A METHOD FOR CONTROLLING A VSC-CONVERTER AND A VSC-CONVERTER



(57) Abstract: A VSC-converter for converting alternating voltage into direct voltage and conversely is controlled so that semiconductor devices of turn-off type connected in anti-parallel with diodes are controlled to be turned on and turned off so that an alternating voltage phase line is alternatively connected to a midpoint (23) of a direct voltage side of the apparatus, the plus pole (7) mad the minus pole (8) of the direct voltage side for generating a train of pulses with determined amplitudes according to a pulse width modulation pattern on the phase output of the apparatus. The midpoint of the direct voltage side is connectable to the phase output through two different so called zero states. The semiconductor devices (13-16, 10, 11) are controlled so that both zero states are each assumed at least once during a half period during which the fundamental frequency component of a voltage set value of the phase output is positive or negative.

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A method for controlling a VSC-converter and a VSC-converter

FIELD OF THE INVENTION AND PRIOR ART

The present invention relates to a method for controlling a VSC-converter for converting alternating voltage into direct voltage and conversely, which comprises a series connection of four units arranged between two poles, a positive and a negative, of a direct voltage side of the converter, each unit comprising a semiconductor device of turn-off type and a diode connected in anti-parallel therewith and being given an order number according to the order thereof in the series connection from the positive to the negative pole, an alternating voltage phase line connected to a first midpoint, called phase output, of the series connection between the second and the third unit, means adapted to provide a midpoint on said direct voltage side between the two poles and put these poles on the same voltage but with opposite signs with respect to the midpoint of the direct voltage side, in which a second midpoint of the series connection between the first and second unit is through a fifth said unit with a diode with the conducting direction with respect to the phase output opposite to the conducting direction of the diode of the second unit connected to the midpoint of the direct voltage side and a third midpoint of the series connection between the third and fourth unit is through a sixth said unit with a diode with the conducting direction with respect to the phase output opposite to that of the diode of the third unit connected to the mid-

point of the direct voltage side, in which the semiconductor devices of the units are controlled to be turned on and turned off so that the alternating voltage phase line is alternatively connected to the midpoint, the plus pole and the minus pole of the direct voltage side for generating a train of pulses with determined amplitudes according to a pulse width modulation pattern on the phase output of the converter, in which the midpoint of the direct voltage side is connectable to the phase output through two different so called zero states, namely a first one in which the second and the fifth unit are in the conducting state, and a second one, in which the third and the sixth unit are in the conducting state, as well as a converter for converting alternating voltage into direct voltage and conversely according to the preamble of the appended device claim.

Thus, the invention relates to conversion of alternating voltage into direct voltage and conversely by utilizing a so-called three level converter of VSC-type (Voltage Source Converter). Such may be used in all types of situations, where direct voltage is to be converted to alternating voltage and conversely, in which examples of such uses are in stations of HVDC-plants (High Voltage Direct Current), in which the direct voltage is normally converted into a three phase alternating voltage or conversely, or in so called back-to-back-stations where the alternating voltage is firstly converted into direct voltage and the latter then into alternating voltage, as well as in SVC's (Static Var Compensator), where the direct voltage side consists of one or more capacitors hanging freely. The alternating current side of the converter could also be connected to an alternating current motor for driving this or to an alternating current generator.

The invention is not restricted to any particular voltage levels of the direct voltage side or magnitude of power to be handled. The formers are advantageously within the interval 1-500 kV.

An advantage of using three level converters instead of two level bridges is that considerably lower frequencies for switching the semiconductor devices of the units according to the pulse width modulation pattern may be used for obtaining a curve shape of the alternating voltage side of a certain quality. The switching losses may hereby be reduced considerably, so that it also gets possible to transfer higher powers through such a three level converter than through a two level bridge, since higher conduction losses may be accepted. Harmonics generated through the pulse width modulation pattern are at the same time reduced.

A three level converter already known is a so-called NPC (Neutral Point Clamped)-converter, in which said fifth and sixth units are replaced by a clamping diode. A disadvantage of such a NPC-converter is that the switching losses will not be distributed evenly on the semiconductor device of the different units (the current valves), but in the case of transferring active power, either by the fact that the converter operates as rectifier or inverter, the switching losses will mainly be generated in the semiconductor devices in the two inner units of the series connection in the rectifier case and the outer ones in the inverter case, i.e. the first and the fourth unit, while when transferring reactive power the great part of the switching and conduction losses will be generated in the semiconductor devices of the two inner units, i.e. the second and the third unit. This means that in a given operation mode some of the semiconductor devices will operate far away from their thermal limit, while other are very close thereto, which restricts the power that may be handled by the converter to an unnecessary extent.

A method and a converter of the type defined in the introduction are already known through the Swedish patent application 9800205-8 of the applicant. The method described therein constitutes a suggestion to a solution to the problem just mentioned of high switching losses restricting the maximum transferable

power through such a converter. The semiconductor devices in the second and third unit, i.e. the units closest to the phase output, are in that method controlled to be turned on and turned off with a considerably higher frequency than the semiconductor devices of the other four units. Since different demands are put on the different semiconductor devices depending upon in which units they are located, they may in such a converter with such a control method be specially designed, so that in the second and third unit semiconductor devices are used which may take higher frequencies especially well, while in the other units semiconductor devices having low conduction losses are advantageously used. It is hereby possible to reduce the total losses in such a converter, especially the total switching losses in the semiconductor devices. Even if such a control method already known is advantageous it requires a special design of the semiconductor devices.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method and a converter of the type defined in the introduction, which make it possible if desired to use substantially identical semiconductor devices in all six units and substantially identical units but obtain a possibility to transfer considerably higher powers, especially when there is a need to use a pulse width modulation pattern with a high pulse frequency, than in a conventional NPC-converter with semiconductor devices of a similar type in the four units thereof. Thus, the invention aims at proposing an advantageous way to utilize the converter with the construction according to the Swedish patent application mentioned above for converting alternating voltage into direct voltage and conversely.

This object is according to the invention obtained by providing a method of the type defined in the introduction, in which the semiconductor devices of the units are controlled so that both zero states are each assumed at least once during a half period

during which the fundamental frequency component of the voltage set value of the phase output is positive or negative. It gets hereby possible to distribute the losses more evenly over at least four of the six units, and the zero state may be changed when desired for obtaining an even distribution of primarily the switching losses, but preferably the sum of the switching and conduction losses on the semiconductor devices of said four units. The semiconductor devices of the remaining two units have normally lower losses than the other four. This constitutes also preferred embodiments of the invention, in which in the case of high switching frequencies, i.e. when the switching losses are dominating, it may be sufficient to distribute the switching losses substantially evenly on the semiconductor devices, but in the case when the conduction losses have a significant importance it is desired to distribute the sum of the switching and conduction losses evenly on the semiconductor devices of the units. It is pointed out that the total losses in the semiconductor devices will be essentially the same as in a conventional NPC-converter, but they will through the method according to the invention be distributed considerably more evenly on the different semiconductor devices, so that it gets possible to transfer a higher power through the converter device controlled according to the method according to the invention without overloading any individual semiconductor device. According to another preferred embodiment of the invention being directed to reactive operation the semiconductor devices of the units are controlled for obtaining said alternative connections to the phase output according to a pattern aiming at reducing the sum of the switching and conduction losses in the semiconductor devices of turn-off type in the second and third unit. The total losses in these semiconductor devices may hereby be reduced with respect to the case of a conventional NPC-converter, so that the current handling ability of the converter may be increased.

According to a preferred embodiment of the invention, within each said half period of the voltage set value of the phase output substantially each time the midpoint of the direct voltage side is to be connected to the phase output the opposite zero state to the one just before is selected. In rectifier and inverter operation a substantially even distribution of the switching losses in the semiconductor devices of turn-off type in the semiconductor devices in four of the six units may hereby take place. In a corresponding way a substantially even distribution of the switching losses in the diode part in the semiconductor devices of four of the six units results in the corresponding way.

According to another preferred embodiment of the invention the semiconductor devices of the units are controlled so that a change between the two zero states is always separated by a connection of the plus or minus pole of the direct voltage side to the phase output. It may hereby be ensured that no extra commutations take place during the dead time that could result if it were changed from one zero state to the other.

According to another preferred embodiment of the invention each time the midpoint of the direct voltage side is to be connected to the phase output the semiconductor devices in the second and fifth unit as well as those in the third and sixth unit are turned on for simultaneously obtaining both zero states. Thus, the invention also comprises a possibility to select both zero states simultaneously, in which the current then may chose the way it "wants". This way of selecting both zero states simultaneously reduces the number of possible states and may hereby simplify the control of the converter. It is pointed out that "turned on" also comprises "leave turned on", i.e. the semiconductor devices of any or some of the units mentioned could be turned on already before the midpoint of the direct voltage side is connected to the phase output.

According to another preferred embodiment of the invention the semiconductor devices of the units are controlled so that a change between connecting the plus and the minus pole to the phase output is always separated by the connection of the midpoint of the direct voltage side according to one of the zero states to the phase output. High switching losses and high voltage jumps otherwise generated on the phase output are hereby avoided. It is then also possible that both zero states are obtained simultaneously according to the previous embodiment.

According to another preferred embodiment of the invention the semiconductor devices of the units are controlled to together alternatively assume four different states, namely a first state for connecting the plus pole of the direct voltage side to the phase output, a second state for connecting the minus pole of the direct voltage side to the phase output and a third and fourth state for connecting the midpoint of the direct voltage to the phase output. By only utilizing four different states of the semiconductor devices of the units, i.e. four different combinations of semiconductor devices turned on and turned off, the very method for controlling the semiconductor devices gets very simple. It is pointed out that in the practice a fifth possible state of course exists in this embodiment, namely when the converter is out of operation and then all the semiconductor devices are turned off. It is here possible to select different combinations for obtaining the first and the second state, in which for obtaining the first state the units 1 and 2 have to be conducting and for obtaining the second state the units 3 and 4 have to be conducting.

By controlling the semiconductor devices of the first and sixth unit in another preferred embodiment of the invention to always assume the same state, turned on or turned off, and the semiconductor devices in the fourth and fifth unit to always assume the same state, turned on or turned off, it will be possible to use the same control signal for the semiconductor devices in the first and sixth unit and in the fourth and fifth unit, respectively, so

that it is in the practice sufficient with four control signals for controlling the sixth units.

According to another preferred embodiment of the invention the semiconductor devices in the first and sixth unit are interlocked with respect to the semiconductor devices in the fourth and fifth unit, so that when the semiconductor devices in any of these unit couples is to be turned on the semiconductor devices of the other unit couple is firstly controlled to be turned off. An undesired fast discharging of any of the capacitors of the DC-side through the first and fifth unit or alternatively through the sixth and fourth unit is hereby prevented. According to another preferred embodiment of the invention the semiconductor devices in the second unit is in a corresponding way interlocked with respect to those in the third unit, in which it is in the same way prevented that an undesired fast discharging of one of the capacitors of the DC-side takes place through either the first, second, third and sixth unit or through the fifth, second, third and fourth unit.

According to another preferred embodiment of the invention are during a first period of time located on both sides of a zero-crossing of the fundamental frequency component of the phase current on the phase output changes between connection of the plus pole and the minus pole, respectively, to the phase output and a zero state thereof carried out so that a large current commutation loop is obtained, and during a second period of time between such first periods of time with a higher absolute value of the phase current the changes last mentioned are carried out so that a small current commutation loop is obtained. The total losses in the converter device may in this way be reduced, since the commutation inductance is kept low when the current intensity is high and a higher inductance is allowed when the current intensity is low, while maintaining the possibility to distribute the switching losses substantially evenly on the semiconductor devices of the different units.

According to preferred embodiments of the invention the first period is in rectifier or inverter operation of the converter selected to extend over a phase angle of the phase current of 50-65°, preferably 55-60°, on each side of said zero-crossing, while the first period is in operation of the converter for transferring mainly reactive power selected to extend over a phase angle of the phase current of 25-45°, preferably 30-35°, on each side of said zero-crossing. It has been found that to the selecting of such a first and second period the maximum power transferable through the converter is increased.

The invention also relates to an apparatus, a computer program and a computer program product according to the corresponding appended claims. It is easily understood that the method according to the invention defined in the appended set of method claims is well suited to be carried out through program instructions from a processor that may be influenced by a computer program provided with the program steps in question. Although not explicitly expressed in patent claims the invention also comprises such apparatuses, computer programs and computer program products combined with a method according to any of the appended method claims.

Further advantages as well as advantageous features of the invention appear from the following description and the other dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

With reference to the appended drawings, below follows a description of preferred embodiments of the invention cited as examples.

In the drawings:

Fig 1 illustrates schematically a converter apparatus of three-level-type of the kind, to which the method according to the invention is applicable,

Fig 2 illustrates schematically how a pulse width modulation pattern is applied on the phase output of a converter according to Fig 1,

Fig 3 is a simplified block diagram illustrating the principle for controlling a converter according to Fig 1 according to the present invention,

Fig 4 illustrates the development of the phase current on the phase output of a converter according to Fig 1 and how according to a preferred embodiment of the invention different control schemes are selected during different periods of time, and

Fig 5 is a diagram illustrating the maximum transferable active and reactive power through a converter according to Fig 1, for methods according to different embodiments of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

The construction of a three-level-converter of the type described in the Swedish patent application 9800205-8 mentioned above of the applicant is illustrated in Fig 1. It is here illustrated how the converter has three so called phase legs 1-3 with a phase output 4-6 each for connecting the alternating voltage side of the converter through a reactor and/or a transformer to a three phase alternating voltage network, but only one of these phase legs will hereinafter be discussed. It is also completely possible that the converter is connected to a one phase alternating voltage network or the alternating voltage side may except from the AC-network be connected to a generator or a motor. The converter is a so called VSC-converter, which has a series connec-

tion of four units S1-S4 arranged between two poles, a positive 7 and a negative 8, of a direct voltage side of the converter, each said unit comprising a semiconductor device 13-16 of turn-off type and a diode 17-20 connected in anti-parallel therewith and are given order numbers according to the order thereof in the series connection from the positive to the negative pole.

Two capacitors 21, 22 connected in series are arranged between said two poles, and a point 23 (the midpoint of the direct voltage side) between these (which it normally the case) is connected to ground 9 through an impedance Z, in which this impedance may vary from zero (= direct grounding of the midpoint of the direct voltage side) to a value X (= impedance grounding of the midpoint of the direct voltage side, through for example a resistance R and an inductance L) up to a value X_{max} (= non-grounded midpoint, where the grounding is only determined by stray capacitances between the midpoint of the direct voltage side and the ground), so that the potentials +U/2 and –U/2 are in this way provided at the respective pole, in which U is the voltage between the two poles 7, 8.

A second midpoint 24 of the series connection between the first and second unit is through a fifth unit S5 with the diode 26 with the conducting direction with respect to the phase output 4 opposite to the conducting direction of the diode of the second unit connected to the midpoint of the direct voltage side and a third midpoint 27 of the series connection between the third and fourth unit is through a sixth said unit S6 with the diode 29 with the conducing direction with respect to the phase output opposite to the diode of the third unit connected to the midpoint of the direct voltage side.

The semiconductor devices of turn-off type of the units S1-S6 may for example be IGBT's or GTO's. Although only one IGBT or GTO per unit has been shown this may stand for a number of IGBT's or GTO's connected in series and controlled simultane-

ously, which is also normally the case, since a comparatively high number of such semiconductor devices are required for holding the voltage to be held by each unit in the blocking state, when the direct voltage side for example has a voltage exceeding 10 kV. Each diode, a so-called freewheeling diode, shown may also stand for a number of diodes connected in series.

The semiconductor devices being parts of the converter are controlled through an arrangement 30 schematically indicated to be turned on and turned off for alternatively connecting the midpoint, the plus pole and the minus pole of the direct voltage side to the phase output of the respective phase leg for generating a train of pulses with determined amplitudes according to a pulse width modulation pattern (PWM) on the phase output. The pulse width modulation frequency is then considerably higher than, advantageously at least 5 times higher, more preferred at least 10 times as high and most preferred at least 20 times as high as the fundamental frequency of the alternating current normally substantially sinusoidal on the phase output of the converter. Thus, the pulse width modulation frequency may preferably be in the order of 1-2 kHz, while the fundamental frequency, i.e. the frequency of the fundamental component of the phase current on the phase output, is typically 50 Hz or 60 Hz. However, when the converter is connected to a generator or motor the frequency of the current may vary within a broad range.

The converter apparatus may be operated in different ways, such as for transferring active power as rectifier or as inverter, or for transferring reactive power, or for transferring a combination of active and reactive power.

The midpoint 23 of the direct voltage side is connectable to the phase output 4 through two different so called zero states, namely a first one, in which the second S2 and the fifth S5 unit are in the conducting state, and a second, in which the third S3 and the sixth S6 unit are in the conducting state. The invention

relates to a method utilizing this option of different zero states for controlling the converter so that preferably the sum of the switching and conduction losses is distributed more evenly over the semiconductor devices of four of the six units, and how such a control may take place according to preferred embodiments of the invention will now be described.

According to a first very preferred embodiment of the invention the semiconductor devices of the units S1-S6 are controlled according to the following scheme:

	S1, S6	S2	S3	S4, S5
+	1	1	0	0
N1	0	1	0	1
N2	1	0	1	0
-	0	0	1	1

Thus, the semiconductor devices of the units are controlled to together alternatively assume four different states, namely a first state (+) for connecting the plus pole of the direct voltage side to the phase output, a second state (-) for connecting the minus pole of the direct voltage side to the phase output and a third (N1) and a fourth (N2) state for connecting the midpoint of the direct voltage side to the phase output. The first and the sixth unit are then controlled to always assume the same state, turned on or turned off, and the semiconductor devices in the fourth and fifth unit are controlled to always assume the same state, turned on or turned off. This means that the semiconductor devices of the first and sixth unit may be controlled through one and the same control signal, and the same is valid for the semiconductor devices of the fourth and fifth unit. According to a very simple embodiment of the invention every second time it is switched between on one hand the positive or negative potential on the phase output and on the other a zero potential thereon the third state is selected as zero

state and every second time the fourth state is selected as zero state, which in rectifier and inverter operation results in a more even distribution of the sum of the losses on the semiconductor devices of the different units, so that the phase current may be increased with respect to a conventional three-level converter of NPC-type before the thermal limit is reached for any semiconductor device and by that a higher power may be handled by the converter.

It is through this control scheme very easy to avoid through-turn on by making an interlocking between the unit couples S1, S6 and S4, S5, so that the semiconductor devices of opposite units have turn-off signals before the semiconductor devices to be turned on receive a turn-on signal. Should such an interlocking not be present and for example S1, S6 be turned on before S4, S5 are turned off when changing from the third state to the first state, the capacitors 21 and 22 will then briefly be short-circuited and high short-circuit currents occur. An interlocking is also made between the second unit S2 and the third unit S3, so that the semiconductor devices of one of these units have a turn-off signal before the semiconductor devices of the other of these units to be turned on receives a turn-on signal. Should namely such an interlocking not be present and for example S2 be turned on before S3 is turned off when changing from the third to the second state, the capacitor 22 will be briefly short-circuited and high short-circuit currents occur.

It is illustrated in Fig 2 what a pulse width modulation pattern may typically look like for a converter of the type shown in Fig 1. The sinus curve 31 shown is then the voltage set value on the phase output 4 of the converter, while it appears that when said set value is positive the plus pole of the direct voltage side and the midpoint 23 thereof are alternatively connected to the phase output, i.e. positive pulses and zero pulses with a varying width are alternating, while when said set value is negative it is alternated between negative pulses and zero pulses. During a half

period p with either positive or negative set value of the voltage each of said two different zero states is according to the invention assumed at least once. This means that at least one of the zero pulse 32, 32'... is due to a zero state differing from at least the one of at least one of the other zero pulses or both zero states are assumed when obtaining the different zero pulses. In the simplified embodiment of the invention described above, in which the zero states change each time, the zero pulses 32 and 32" would correspond to the same zero state, while the pulses 32' and 32'" would correspond to the same, but the other zero state.

It is very schematically illustrated in Fig 3 how the control through the control arrangement 30 may in the practice be carried out. A reference value corresponding to the voltage set value of the phase output is at 33 received by a pulse width modulation generator 34, which elaborates the pulse width modulation pattern shown in Fig 2 and sends a pulse width modulation signal on the output 35 thereof, which orders a positive, a negative or a zero pulse on the phase output, to a zero state selector 36, which sends a pulse width modulation signal containing information also about which zero state is to be selected when a zero pulse shall be put on the phase output, to a means 37 for controlling the semiconductor devices of the different units S1-S6 to be turned on or turned off, which is illustrated through the six arrows 38 to the semiconductor devices.

According to another preferred embodiment of the invention it is intended to carry out changes between connecting the plus pole and the minus pole, respectively, to the phase output and a zero state thereof during a first time period T1 (see Fig 4) located on both sides of a zero-crossing 0 of the fundamental frequency component of the phase current I, so that a large current commutation loop is obtained and during a second time period T2 between such first time periods with a higher absolute value of the phase current the changes last mentioned are carried out so

that a small current commutation loop is obtained. In the control scheme as above with the four different states this means that during the first time period T1 it is for a positive voltage set value of the phase output changed between the first and the fourth state and for a negative voltage set value of the phase output between the second and the third state, and during the second time period T2 it is at a positive voltage set value of the phase output changed between the first and the third and at a negative voltage set value of the phase output between the second and the fourth state. By actually changing control scheme in this way depending upon how high the fundamental frequency component of the phase current is the inductive commutation losses of the converter apparatus may be kept down, since the large commutation loop is only used when the current is low, but an even distribution of the sum of the losses during a half period of the fundamental component of the phase current on the semiconductor devices of the different units may nevertheless take place. The losses may in this way be reduced somewhat further with respect to the simplified control scheme described above, since the large commutation loop is sometimes also selected for high currents. Thus, starting from a connection of the plus pole to the phase output through conduction of S1 and S2 a small commutation loop is for example obtained when subsequently the midpoint 23 is connected to the phase output to S5 and S2 and a large commutation loop is obtained through connection of the midpoint 23 through S6 and S3.

Besides the control scheme described there are many other control schemes able to deliver a result being just as good but are more or less complicated to achieve. An example of such a control scheme according to another embodiment of the invention for controlling a converter according to Fig 1 through eight different states is shown below, of which the states 1-4 according to a first control scheme are used during the second time period mentioned above and the fifth to the eighth state

according to the second control scheme during said first time period.

Control scheme 1

	S1	S2	S3	S4	S5	S6
+	1	1	0	0	0	0
N1	0	1	0	0	1	0
N2	0	0	1	0	0	1
-	0	0	1	1	0	0

Control scheme 2

	S1	S2	S3	S4	S5	S6
+	1	1	0	0	0	1
N1	1	0	1	0	0	1
N2	0	1	0	1	1	0
-	0	0	1	1	1	0

It may in the following way be understood that also other control schemes may be achieved: for obtaining the +-state the first and the second unit have to be conducting, but it is optional to have the semiconductor device in the sixth unit turned on or not. Similarly the third and fourth units have to be conducting for obtaining the —-state, but it does not matter if the semiconductor device of the fifth unit is turned on or not. The zero state may be obtained by having the semiconductor device of the second and fifth unit turned on, but it is then optional to have the semiconductor device in the fourth unit turned on. Likewise, another zero state may be obtained by having the semiconductor device in the third and sixth unit turned on, but it is optional to have the semiconductor device in the first unit turned on. It appears from this that many different control schemes are possible, but the

control scheme described previously with only four states is easier to implement.

It is illustrated in Fig 5 in a P- (active power)- Q (reactive power)-diagram what the maximum allowed phase current looks like in different types of operation for the case of the simplified control scheme as above with change of zero state every second time (curve A) and the control scheme as above while adapting the current commutation loops to the magnitude of the phase current (curve B). Inverter operation and rectifier operation are indicated through V and L, respectively. It means in this case that when reactive power is transferred it makes the most sense to use a change between different control schemes depending upon the magnitude of the phase current. It has also turned out that the optimum phase angle for the first time period is about ±30° from the zero-crossing of the fundamental component of the phase current at reactive current and about ±60° from the zero-crossing of the fundamental component of the phase current at active current, and it is accordingly advantageous to be located between these values at active and reactive current for obtaining a distribution of losses being as even as possible on the semiconductor devices of the different units.

Calculations have shown that the phase current may typically increase by a factor of 1.3-1.5 by using the methods according to the embodiments of the invention described above in comparison with the current thermally limited allowed in a corresponding NPC-converter. This factor is strongly depending upon the proportion of the switching losses with respect to the conduction losses. However, also the conduction losses are by this control method redistributed in an advantageous way.

The invention is of course not in any way restricted to the preferred embodiments described above, but many possibilities to modifications thereof will be apparent to a person with skill in

the art without departing from the basic idea of the invention as defined in the claims.

Many other possibilities to control schemes utilizing the basic idea of the invention will be apparent to persons with skill in the art.

It is pointed out that in the case of a voltage set value being non-sinusoidal a plurality of changes of the sign of the voltage set value may occur during a half period of the fundamental frequency component of the phase current, and this is the reason for relating the half period in the independent patent claim also with respect to the time length thereof to said fundamental frequency component, since it is during this half period the two zero states have to be assumed at least once each.

Claims

1. A method for controlling a VSC-converter for converting alternating voltage into direct voltage and conversely, which comprises a series connection of four units (S1-S4) arranged between two poles, a positive (7) and a negative (8), of a direct voltage side of the converter, each unit comprising a semiconductor device (13-16) of turn-off type and a diode (17-20) connected in anti-parallel therewith and being given an order number according to the order thereof in the series connection from the positive to the negative pole, an alternating voltage phase line connected to a first midpoint, called phase output (4), of the series connection between the second and the third unit, means (9) adapted to provide a midpoint (23) on said direct voltage side between the two poles and put these poles on the same voltage but with opposite signs with respect to the midpoint of the direct voltage side, in which a second midpoint of the series connection between the first and second unit is through a fifth said unit (S5) with a diode (26) with the conducting direction with respect to the phase output (4) opposite to the conducting direction of the diode of the second unit connected to the midpoint (23) of the direct voltage side and a third midpoint (27) of the series connection between the third and fourth unit is through a sixth said unit (S6) with a diode (29) with the conducting direction with respect to the phase output opposite to that of the diode of the third unit connected to the midpoint of the direct voltage side, in which the semiconductor devices of the units are controlled to be turned on and turned off so that the alternating voltage phase line is alternatively connected to the midpoint (23), the plus pole (7) and the minus pole (8) of the direct voltage side for generating a train of pulses with determined amplitudes according to a pulse width modulation pattern on the phase output of the converter, in which the midpoint of the direct voltage side is connectable to the phase output through two different so called zero states, namely a first one in which the second and the fifth unit are in

the conducting state, and a second one, in which the fifth and the sixth unit are in the conducting state, ***characterized*** in that the semiconductor devices of the units are controlled so that both zero states are assumed at least once each during a half period during which the fundamental frequency component of a voltage set point of the phase output is positive or negative.

2. A method according to claim 1, ***characterized*** in that the semiconductor devices of the units (S1-S6) are controlled for obtaining said alternative connections to the phase output (4) according to a pattern that in operation as rectifier or inverter distributes the switching losses substantially evenly on the semiconductor devices of turn-off type of at least four of the sixth units.

3. A method according to claim 1, ***characterized*** in that the semiconductor devices of the units (S1-S6) are controlled for obtaining said alternative connections to the phase output (4) according to a pattern that in operation as rectifier or inverter distributes the sum of the switching and the conduction losses substantially evenly on the semiconductor devices of turn-off type of at least four of the sixth units.

4. A method according to claim 1, ***characterized*** in that the semiconductor devices of the units (S1-S6) are controlled for obtaining said alternative connections to the phase output (4) according to a pattern, which in reactive operation aims at reducing the sum of the switching and conduction losses in the semiconductor device of turn-off type of the second and third unit.

5. A method according to any of claims 1-4, ***characterized*** in that within each said half period of the fundamental frequency component of the voltage setpoint of the phase output (4) more than a third of the times the midpoint (23) of the direct voltage

side shall be connected to the phase output (4) the zero state being opposite to the preceding zero state is selected.

6. A method according to any of claims 1-4, ***characterized*** in that within each said half period of the fundamental frequency component of the voltage setpoint of the phase output (4) substantially each time the midpoint (23) of the direct voltage side shall be connected to the phase output (4) the zero state being opposite to the preceding zero state is selected.

7. A method according to any of claims 1-6, ***characterized*** in that the semiconductor devices of the units are controlled so that a change between the two zero states (N1, N2) is always separated by a connection of the plus or minus pole of the direct voltage side to the phase output.

8. A method according to any of claims 1-3, ***characterized*** in that at least one time during each said half period of the fundamental frequency component of the voltage setpoint of the phase output when the midpoint (23) of the direct voltage side shall be connected to the phase output the semiconductor devices in the second and the fifth unit (S2, S5) as well as those in the third and sixth unit (S3, S6) are turned on for simultaneously obtaining both zero states.

9. A method according to claim 8, ***characterized*** in that each time the midpoint (23) of the direct voltage side shall be connected to the phase output the semiconductor devices in the second and fifth unit (S2, S5) as well as those in the third and sixth unit (S3, S6) are tuned on for simultaneously obtaining both zero states.

10. A method according to any of claims 1-9, ***characterized*** in that the semiconductor devices of the units are controlled so that a change between connecting the plus and minus pole to the phase output is always separated by a connection of the

midpoint of the direct voltage side according to one of the zero states (N1, N2) to the phase output.

11. A method according to claim 10, ***characterized*** in that the semiconductor devices of the units (S1-S6) are controlled to together alternatively assume four different states, namely a first state for connecting the plus pole of the direct voltage side to the phase output, a second state for connecting the minus pole of the direct voltage side to the phase output and a third and fourth state for connecting the midpoint of the direct voltage side to the phase output.

12. A method according to claim 11, ***characterized*** in that the semiconductor devices of the first (S1) and the sixth (S6) unit are controlled to always assume the same state, turned on or turned off, and that the semiconductor devices in the fourth (S4) and the fifth (S5) unit are controlled to always assume the same state, turned on or turned off.

13. A method according to claim 12, ***characterized*** in that the semiconductor devices of the first and the sixth unit are controlled by sending the same control signal thereto and those of the fourth and the fifth unit are controlled by sending the same control signal thereto.

14. A method according to any of claims 11-13, ***characterized*** in that the first state is obtained by controlling the semiconductor devices in the first, second and sixth unit (S1, S2, S6) to be turned on and those in the third, fourth and fifth unit (S3, S4, S5) to be turned off, the second state by controlling the semiconductor devices in the third, fourth and fifth unit to be turned on and those in the first, second and sixth unit to be turned off, the third state (N1) by controlling the semiconductor devices in the second, fourth and fifth unit to be turned on and those in the first, third and sixth unit to be turned off, and the fourth state (N2) by controlling the semiconductor devices in the first, third

and sixth unit to be turned on and those in the second, fourth and fifth unit to be turned off.

15. A method according to any of claims 11-14, ***characterized*** in that the semiconductor devices in the first (S1) and the sixth (S6) unit are interlocked with respect to the semiconductor devices in the fourth (S4) and fifth (S5) unit, so that when the semiconductor devices of any of these couples of units is to be turned on the semiconductor devices of the other couple of units are firstly controlled to be turned off.

16. A method according to any of claims 11-15, ***characterized*** in that the semiconductor devices in the second unit (S2) are interlocked with respect to the semiconductor devices in the third unit (S3), so that when the semiconductor devices of any of these units are to be tuned on the semiconductor devices of the opposite of these two units are firstly controlled to be turned off.

17. A method according to claim 1, ***characterized*** in that the semiconductor devices of the units are controlled to together alternatively assume eight different states, namely four states according to a first control scheme in the form of a first state for connecting the plus pole of the direct voltage side to the phase output, a second state for connecting the minus pole of the direct voltage side to the phase output and a third (N1) and a fourth (N2) state for connecting the midpoint (23) of the direct voltage side to the phase output, as well as four states according to a second control scheme in the form of a fifth state for connecting the plus pole of the direct voltage side to the phase output, a sixth state for connecting the minus pole of the direct voltage side to the phase output and a seventh (N1) and an eighth state (N2) for connecting the midpoint of the direct voltage side to the phase output.

18. A method according to claim 17, ***characterized*** in that in the first state the semiconductor devices in the first (S1) and the

second (S2) units are controlled to be turned on and those in the third (S3), fourth (S4), fifth (S5) and sixth (S6) units to be turned off, in the second state the semiconductor devices in the third and fourth unit to be turned on and those in the first, second, fifth and sixth unit to be turned off, in the third state the semiconductor devices in the second and fifth unit to be turned on and those in the first, third, fourth and sixth unit to be turned off, in the fourth state the semiconductor devices in the third and sixth unit to be turned on and those in the first, second, fourth and fifth unit to be turned off, in the fifth state the semiconductor devices in the first, second and sixth unit to be turned on and those in the third, fourth and fifth unit to be turned off, in the sixth state the semiconductor devices in the third, fourth and fifth unit to be turned on and those in the first, second and sixth unit to be turned off, in the seventh state the semiconductor device in the first, third and sixth unit to be turned on and those in the second, fourth and fifth unit to be turned off, and in the eighth state the semiconductor devices in the second, fourth and fifth unit to be turned on and those in the first, third and sixth unit to be turned off.

19. A method according to any of claims 8-18, ***characterized*** in that during a first period of time (T1) located on both sides of a zero-crossing (0) of the fundamental frequency component of the phase current (I) on the phase output (4) changes between connection of the plus pole and the minus pole, respectively, to the phase output and a zero state thereof are carried out so that a large current commutation loop is obtained and during a second period of time (T2) between such first periods of time with a higher absolute value of the phase current the changes last mentioned are carried out so that a small current commutation loop is obtained.

20. A method according to claim 19, ***characterized*** in that in a rectifier or inverter operation of the converter the first period (T1) is selected to extend over a phase angle of the fundamental

frequency component of the phase current of 50-65°, preferably 55-60°, on each side of said zero-crossing.

21. A method according to claim 19, ***characterized*** in that in operation of the converter for transferring mainly reactive power the first period (T1) is selected to extend over a phase angle of the fundamental frequency component of the phase current of 25-40°, preferably 30-35°, on each side of said zero-crossing.

22. A method according to claims 11 and 19, ***characterized*** in that during the first period of time (T1) it is changed between the first and fourth (N2) state when the voltage set value of the phase output is positive and between the second and third (N1) state when the voltage set value of the phase output is negative, and during the second period of time (T2) it is changed between the first and third state when the voltage set value of the phase output is positive and between the second and fourth state when the voltage set value of the phase output is negative.

23. A method according to claims 18 and 19, ***characterized*** in that during the first period of time (T1) the second control scheme is selected, according to which it is changed between the fifth, sixth, seventh and eighth state by changing between the fifth and seventh state when the phase current is positive and changing between the sixth and eighth state when the phase current is negative, and during the second period of time (T2) the first control scheme is selected, according to which it is changed between the first, second, third and fourth state by changing between the first and third state when the phase current is positive and between the second and fourth state when the phase current is negative.

24. A method according to any of the preceding claims, ***characterized*** in that it is semiconductor devices (13-16, 10, 11) in the form of IGBT's (Insulated Gate Bipolar Transistors) that are controlled to be turned on and turned off.

25. A method according to any of claims 1-23, ***characterized*** in that it is semiconductor devices (13-16, 10, 11) in the form of GTO's (Gate Turn-Off thyristors) that are controlled to be turned on and turned off.

26. A method according to any of the preceding claims, ***characterized*** in that it is a VSC-converter with a direct voltage side formed by a direct voltage network for transferring high voltage direct current (HVDC) and an alternating voltage phase line belonging to an alternating voltage network that is controlled.

27. A method according to any of claims 1-25, ***characterized*** in that it is two VSC-converters of a back-to-back-station with the direct voltage sides thereof connected to one and the same or an alternating voltage network each and having the direct voltage sides thereof connected to each other that are controlled.

28. A method according to any of claims 1-25, ***characterized*** in that it is a VSC-converter being included in a SVC (Static Var Compensator) with the direct voltage side formed by capacitors hanging freely and the alternating voltage phase line belonging to an alternating voltage network that is controlled.

29. A method according to any of claims 1-25, ***characterized*** in that it is a VSC-converter with an alternating voltage side connected to an alternating current motor that is controlled.

30. A method according to any of claims 1-25, ***characterized*** in that it is a VSC-converter with the alternating voltage side connected to an alternating current generator that is controlled.

31. A VSC-converter for converting alternating voltage into direct voltage and conversely, which comprises a series connection of four units (S1-S4) arranged between two poles, a positive (7) and a negative (8), of a direct voltage side of the converter,

which each comprises a semiconductor device (13-16) of turn-off type and a diode (17-20) connected in anti-parallel therewith and are given order numbers according to the order thereof in the series connection from the positive to the negative pole, an alternating voltage phase line connected to a first midpoint, called phase output (4), of the series connection between the second and third unit, means (9) adapted to provide a midpoint (23) on said direct voltage side between the two poles and put these poles on the same voltage but with opposite signs with respect to the midpoint of the direct voltage side, in which a second midpoint (24) of the series connection between the first and second unit is through a fifth (S5) said unit with the diode (26) with the conducting direction with respect to the phase output opposite to the conducting direction of the diode of the second unit connected to the midpoint of the direct voltage side and a third midpoint (27) of the series connection between the third and fourth unit is through a sixth (S6) said unit with the diode with the conducting direction with respect to the phase output opposite to that of the diode of the third unit connected to the midpoint of the direct voltage side, in which the converter also comprises an arrangement (30) adapted to control the semiconductor devices of the units to be turned on and turned off for alternatively connecting the alternating voltage phase line to the midpoint (23), the plus pole (7) and the minus pole (8) of the direct voltage side for generating a train of pulses with determined amplitudes according to a pulse width modulation pattern on said phase output (4), and in which the midpoint of the direct voltage side is connectable to the phase output through two different so called zero states, namely a first one, in which the second and fifth unit are in the conducting state, and a second, in which the third and the sixth unit are in the conducting state, ***characterized*** in that the arrangement (30) is adapted to control the semiconductor devices of the units so that both zero states are each assumed at least once during a half period during which the fundamental frequency component

of a voltage set value of the phase output is positive or negative.

32. An apparatus for controlling a VSC-converter for converting alternating voltage into direct voltage and conversely, which converter comprises a series connection of four units (S1-S4) arranged between two poles, a positive (7) and a negative (8), of a direct voltage side of the converter, which each comprises a semiconductor device (13-16) of turn-off type and a diode (17-20) connected in anti-parallel therewith and are given order numbers according to the order thereof in the series connection from the positive to the negative pole, an alternating voltage phase line connected to a first midpoint, called phase output (4), of the series connection between the second and third unit, means (9) adapted to provide a midpoint (23) on said direct voltage side between the two poles and put these poles on the same voltage but with opposite signs with respect to the midpoint of the direct voltage side, in which a second midpoint (24) of the series connection between the first and second unit is through a fifth (S5) said unit with the diode (26) with the conducting direction with respect to the phase output opposite to the conducting direction of the diode of the second unit connected to the midpoint of the direct voltage side and a third midpoint (27) of the series connection between the third and fourth unit is through a sixth (S6) said unit with the diode with the conducting direction with respect to the phase output opposite to that of the diode of the third unit connected to the midpoint of the direct voltage side, which apparatus comprises a program module comprising at least one processor adapted to carry out program instructions to control the semiconductor devices of the units so that the alternating voltage phase line is alternatively connected to the midpoint (23), the plus pole (7) and the minus pole (8) of the direct voltage side for generating a train of pulses with determined amplitudes according to a pulse width modulation pattern on the phase output of the converter, in which the midpoint of the direct voltage side is connectable to the phase

output through two different so called zero states, namely a first one in which the second and fifth units are in conducting state, and a second one, in which the third and sixth units are in a conducting state, and to control the semiconductor devices of the units so that both zero states are assumed each at least once during a half period during which the fundamental frequency component of a voltage set value of the phase output is positive or negative.

33. A computer program for controlling a VSC-converter for converting alternating voltage into direct voltage and conversely, in which the computer program comprises instructions for influencing a processor to cause a series connection of four units (S1-S4) arranged between two poles, a positive (7) and a negative (8) of the direct voltage side of the converter, which each comprises a semiconductor device (13-16) of turn-off type and a diode (17-20) connected in anti-parallel therewith and are given order numbers according to the order thereof in the series connection from the positive to the negative pole, an alternating voltage phase line connected to a first midpoint, called phase output (4), of the series connection between the second and third unit, means (9) adapted to provide a midpoint (23) on said direct voltage side between the two poles and put these poles on the same voltage but with opposite signs with respect to the midpoint of the direct voltage side, in which a second midpoint (24) of the series connection between the first and second unit is through a fifth (S5) said unit with the diode (26) with the conducting direction with respect to the phase output opposite to the conducting direction of the diode of the second unit connected to the midpoint of the direct voltage side and a third midpoint (27) of the series connection between the third and fourth unit is through a sixth (S6) said unit with the diode (29) with the conducting direction with respect to the phase output opposite to that of the diode of the third unit connected to the midpoint of the direct voltage side, in which the computer program comprises instructions for influencing a processor to cause control

of the semiconductor devices of the units so that the alternating voltage phase line is alternatively connected to the midpoint (23), the plus pole (7) and the minus pole (8) of the direct voltage side for generating a train of pulses with determined amplitudes according to a pulse width modulation pattern on the phase output (4) of the converter, in which the midpoint of the direct voltage side is connectable to the phase output through two different so called zero states, namely a first one in which the second and the fifth units are in the conducting state, and a second one, in which the third and the sixth units are in the conducting state, and control of the semiconductor devices of the units so that both zero states are assumed each at least once during a half period during which the fundamental frequency component of a voltage set value of the phase output is positive or negative.

34. A computer program according to claim 33 provided at least partially over a network such as the Internet.

35. A computer program product directly loadable into the internal memory of a digital computer and comprising software code portions for carrying out the steps according to any of the claims 1-30 and the product is run on a computer.

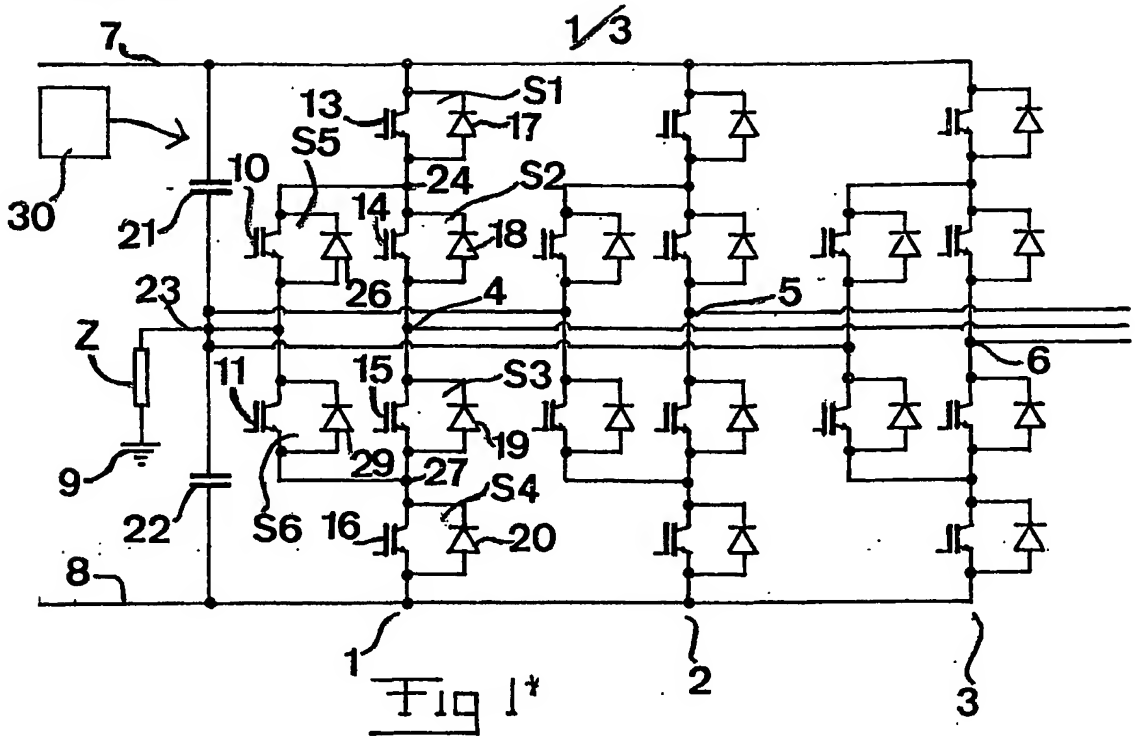

Fig 1*

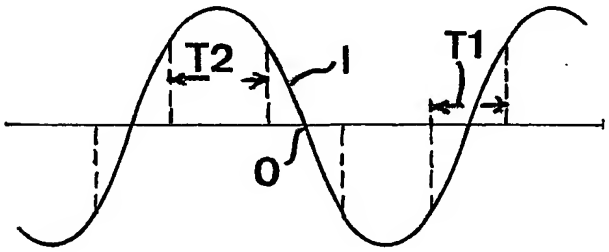

Fig 4

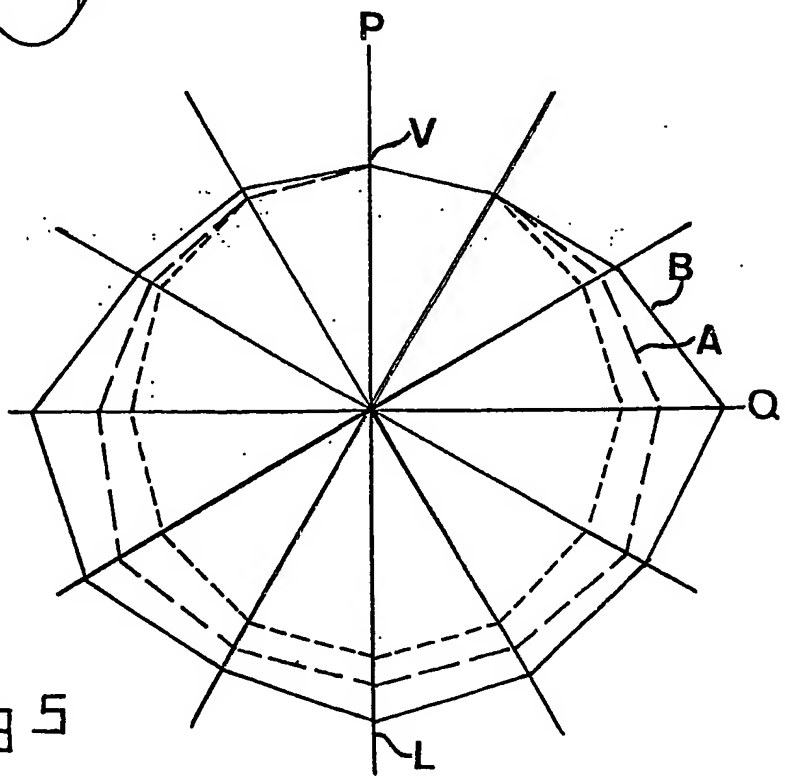

Fig 5

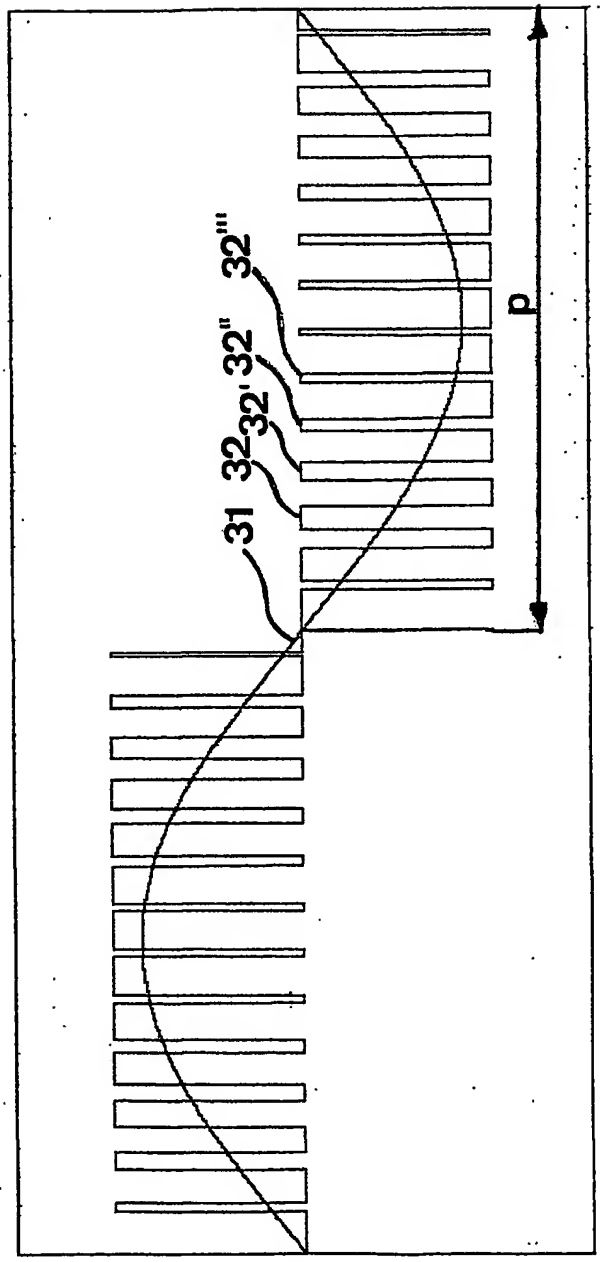

Fig 2

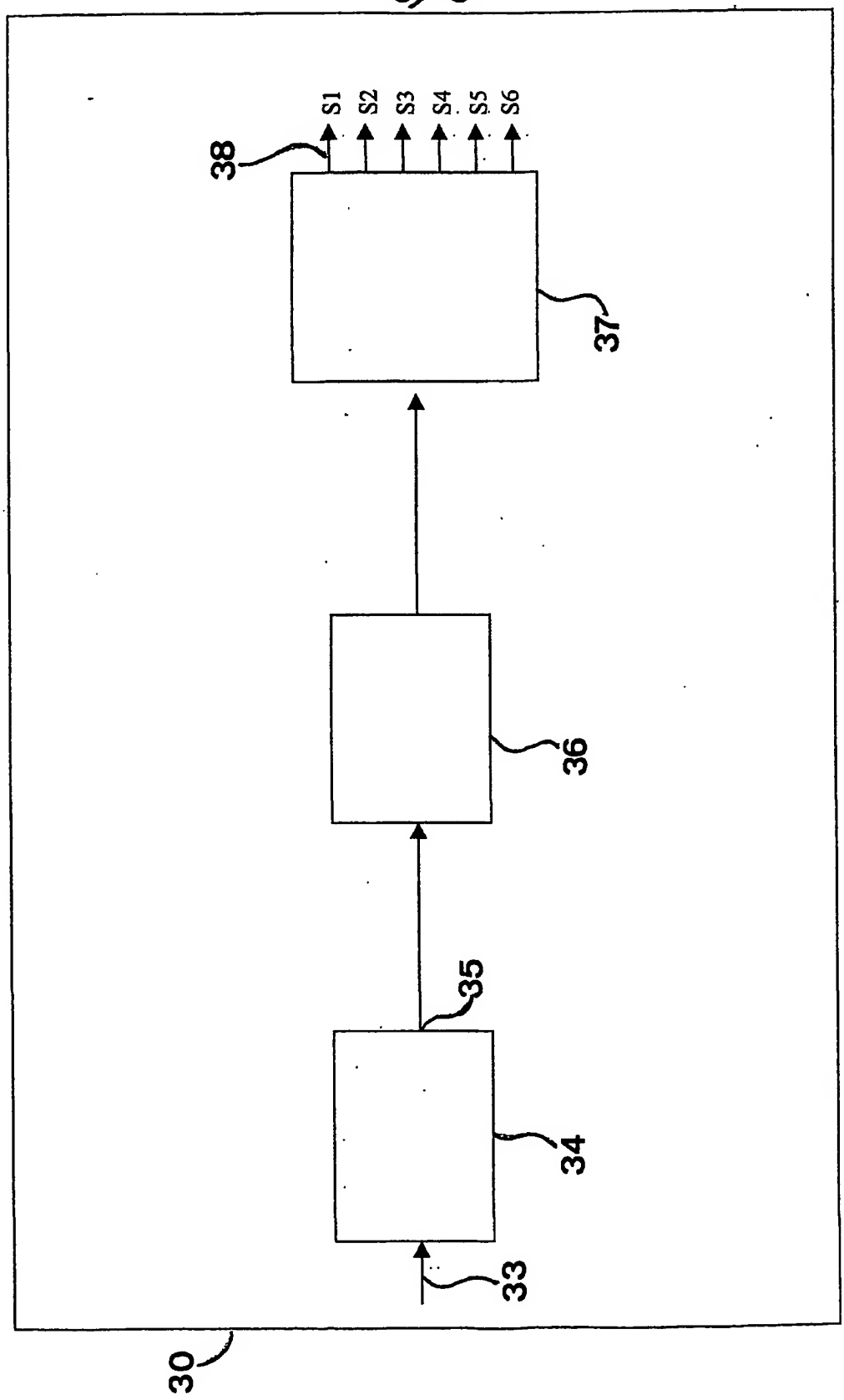

Fig 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 01/02146

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H02M 7/48
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 9940676 A1 (ASEA BROWN BOVERI AB), 12 August 1999 (12.08.99), page 12, line 8 - line 11, figure 3, abstract --	1-35
A	US 5621634 A (SHINJI SATO), 15 April 1997 (15.04.97), figure 1 --	1-35
A	US 5684688 A (DIDIER G. ROUAUD ET AL), 4 November 1997 (04.11.97), figure 6 --	1-35
A	US 4432032 A (RICHARD H. BAKER ET AL), 14 February 1984 (14.02.84), figure 5 --	1-35

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 January 2002	22 -01- 2002
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Tomas Erlandsson/MN Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

Information on patent family members

06/11/01

International application No.
PCT/SE 01/02146

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9940676 A1	12/08/99	DE 19882118 T	27/01/00
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		FI 991882 A	03/09/99
		GB 2335016 A	08/09/99
		GB 9912897 D	00/00/00
		NO 994285 A	03/09/99
		SE 511219 C	23/08/99
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US 4432032 A	14/02/84	NONE	